Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-12 (canceled)

Claim 13 (currently amended): Processor system,

with a processor unit for executing instructions filed in a program memory,

whereby the processor unit comprises instruction read out means for reading out an instruction from the program memory, and instruction decoding means for decoding the instruction and instruction executing means for executing the instruction,

whereby the instruction executing means comprise a plurality of executing units operable in parallel for parallel execution of various instructions, and the instruction read out means and the instruction decoding means ~~(3)~~ are jointly provided for all executing units, ~~and~~

~~wherein~~ whereby ~~an~~ a first executing unit of the instruction executing ~~meansis~~ means is connected to a first databus and a second executing unit is connected to a second databus whereby the transmission rate of the first databus is lower than the transmission rate of the second databus, and

whereby the first executing unit of the instruction executing means is designed to execute all types of instructions of a set of instructions of the processor system, while the second executing unit is designed to execute only one special type of instructions of the instruction set of the processor system.

Claim 14 (previously presented): Processor system according to claim 13, wherein temporary storage means for storing information required for executing the instruction to be carried out by the particular executing unit are associated with each executing unit.

Claims 15-16 (canceled)

Claim 17 (currently amended): Processor system according to claim ~~16~~13, wherein the second executing unit is designed to execute only an instruction to move a data block.

Claim 18 (previously presented): Processor system according to claim 14 wherein information stored in the temporary storage means associated with the second executing unit comprises a storage or loading address of the datablock to be stored or loaded, the amount of data elements of the datablock to be moved, an offset value, with which the datablock has to be stored or read and/or control information, which specifies whether the instruction to be carried out concerns a storage or read instruction.

Claim 19 (currently amended): Processor system according to claim ~~15~~13 wherein the processor unit is designed in such a way that the path leading to the first executing unit is temporarily deactivated by the instruction read out means via the instruction decoding means, if momentarily no instruction has to be executed by the first executing unit.

Claim 20 (previously presented): Processor system according to claim 13 wherein the processor system is intended for processing telecommunications protocols, and the first databus is intended for processing header data of the telecommunications protocols, while the second databus is intended for fast transfer of payload data.

Claim 21 (previously presented): Processor system according to claim 13 wherein a data memory of the processor system is connected to the first databus, and at least one input and/or output port and/or at least one register or buffer is connected to the second databus.

Claim 22 (previously presented): Processor system according to claim 20 wherein the input and/or output port connected to the second databus is connected to a transmitter and/or receiver unit of a communication transmitter, and the register or buffer connected to the second databus is provided for temporary storage of a bitstream to be transmitted or received by the communication transmitter.

Claim 23 (currently amended): Processor system according to claim ~~15~~13, wherein the executing unit of the instruction executing means connected to the first databus corresponds to the first executing unit and the executing unit connected to the second databus corresponds to the second executing unit.

Claim 24 (previously presented): Processor system according to claim 23 wherein the first executing unit is also connected to the second databus, so that it can also access the second databus, while the second executing unit is only connected to the second databus.